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PTO/SB/05 (4/98)
Approved for use through 09/30/2000 OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MI30-052
First Inventor or Application Identifier	Ammar Derraa
Title	Cathod Assemblies (as amended)
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original and a duplicate for fee processing)

2. [X] Specification [Total Pages 25]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 3]

4. Oath or Declaration [Total Pages 2]
a. [ ] Newly executed (original or copy)
b. [X] Copy from a prior application (37 C.F.R. § 1.63(d))
(for continuation/divisional with Box 16 completed)
i. [ ] DELETION OF INVENTOR(S)
Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).

5. [ ] Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [X] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [X] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
15. [X] Other: Check

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [X] Divisional [ ] Continuation-in-part (CIP) of prior application No. 09/251,262
Prior application information: Examiner D. Hardy Group / Art Unit: 2815

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* **021567** *(Insert Customer No. or Attach bar code label here)* or [ ] *Correspondence address below*

Name					
Address					
City		State		Zip Code	
Country		Telephone		Fax	

Name (Prnt/Type)	David G. Latwesen, Ph.D.	Registration No. (Attorney/Agent)	38,533
Signature		Date	11/13/00

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

PTO/SB/17 (2/98)
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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

EL465852811

FEE TRANSMITTAL

Patent fees are subject to annual revision on October 1.
These are the fees effective October 1, 1997.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.
See 37 C.F.R. §§1.27 and 1.28.

TOTAL AMOUNT OF PAYMENT ($) 710.00

Complete if Known	
Application Number	PRIORITY: 09/251,262
Filing Date	PRIORITY: February 16, 1999
First Named Inventor	Ammar Derraa
Examiner Name	PRIORITY: D. Hardy
Group / Art Unit	PRIORITY: 2815
Attorney Docket No.	MI30-052

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 23-0925
Deposit Account Name: Wells, St. John et al.

[X] Charge Any Additional Fee Required Under 37 C.F.R. §§ 1.16 and 1.17
[ ] Charge the Issue Fee Set in 37 C.F.R §1.18 at the Mailing of the Notice of Allowance

2. [X] **Payment Enclosed:**
[X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	790	201	395	Utility filing fee	710.00
106	330	206	165	Design filing fee	
107	540	207	270	Plant filing fee	
108	790	208	395	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below	Fee Paid
Total Claims 10	-20** = 0	X		= 0
Independent Claims 1	- 3** = 0	X		= 0
Multiple Dependent				= 0

***or number previously paid, if greater; For Reissues, see below*

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	22	203	11	Claims in excess of 20
102	82	202	41	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	82	209	41	** Reissue independent claims over original patent
110	22	210	11	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	0.00
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	0.00
139	130	139	130	Non-English specification	0.00
147	2,520	147	2,520	For filing a request for reexamination	0.00
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	0.00
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	0.00
115	110	215	55	Extension for reply within first month	0.00
116	400	216	200	Extension for reply within second month	0.00
117	950	217	475	Extension for reply within third month	0.00
118	1,510	218	755	Extension for reply within fourth month	0.00
128	2,060	228	1,030	Extension for reply within fifth month	0.00
119	310	219	155	Notice of Appeal	0.00
120	310	220	155	Filing a brief in support of an appeal	0.00
121	270	221	135	Request for oral hearing	0.00
138	1,510	138	1,510	Petition to institute a public use proceeding	0.00
140	110	240	55	Petition to revive - unavoidable	0.00
141	1,320	241	660	Petition to revive - unintentional	0.00
142	1,320	242	660	Utility issue fee (or reissue)	0.00
143	450	243	225	Design issue fee	0.00
144	670	244	335	Plant issue fee	0.00
122	130	122	130	Petitions to the Commissioner	0.00
123	50	123	50	Petitions related to provisional applications	0.00
126	240	126	240	Submission of Information Disclosure Stmt	0.00
581	40	581	40	Recording each patent assignment per property (times number of properties)	0.00
146	790	246	395	Filing a submission after final rejection (37 CFR 1.129(a))	0.00
149	790	249	395	For each additional invention to be examined (37 CFR 1.129(b))	0.00
Other fee (specify) _____					0.00
Other fee (specify) _____					0.00

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0.00

SUBMITTED BY

				Complete (if applicable)	
Typed or Printed Name	David G. Latwesen, Ph.D.			Reg. Number	38,533
Signature		Date	11/13/00	Deposit Account User ID	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

priority Application Serial No. 09/251,262
priority Filing Date ..... February 16, 1999
Inventor ..... Ammar Derraa
Assignee ..... Micron Technology, Inc.
priority Group Art Unit 2815
priority Examiner ..... D. Hardy
Attorney's Docket No. MI30-052
Title: Cathode Assemblies

PRELIMINARY AMENDMENT

To: Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

From: David G. Latwesen, Ph.D. (Tel. 509-624-4276; Fax 509-838-3424)
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828

AMENDMENTS

In the Specification

Replace the title with --Cathode Assemblies--.

At p. 1, before the "Technical Field" section, insert

--**RELATED PATENT DATA**

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/251,262, which was filed on February 16, 1999.--.

Amended Claims

Cancel claims 1-52.

REMARKS

Claims 1-52 are canceled, leaving claims 53-62 pending in the application. Applicant requests substantive examination of the pending claims.

Respectfully submitted,

Dated: 11/13/00 By: _____

David G. Latwesen, Ph.D.
Reg. No. 38,533

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Methods Of Treating Regions Of Substantially Upright Silicon-comprising Structures, Methods Of Treating Silicon-comprising Emitter Structures, Methods Of Forming Field Emission Display Devices, And Cathode Assemblies

* * * * *

INVENTOR

Ammar Derraa

ATTORNEY'S DOCKET NO. MI30-036

Methods Of Treating Regions Of Substantially Upright Silicon-comprising Structures, Methods Of Treating Silicon-comprising Emitter Structures, Methods Of Forming Field Emission Display Devices, And Cathode Assemblies

PATENT RIGHTS STATEMENT

This invention was made with Government support under Contract No. DABT63-97-C-0001 awarded by Advanced Research Projects Agency (ARPA). The Government has certain rights in this invention.

TECHNICAL FIELD

The invention pertains to methods of treating substantially upright silicon-comprising structures, such as, for example, methods of treating silicon-comprising emitter structures. In particular aspects, the invention pertains to methods of forming field emission display devices. In other particular aspects, the invention pertains to cathode assemblies.

BACKGROUND OF THE INVENTION

Silicon-comprising field emitters are currently being designed and incorporated into field emission display devices, and show promise as candidates for electron sources in vacuum microelectronic devices. It is generally desirable to fabricate the emitters to have tips that are as sharp as possible, as such can improve control of electron emission from the tips. For instance, clarity, or resolution, of a field emission display is a function of, among other things, emitter tip sharpness. As sharper

emitter tips can produce higher resolution displays than less sharp emitter tips, numerous methods have been proposed for fabrication of very sharp emitter tips (i.e., emitter tips having tip radii of 100 nanometers or less).

Fabrication of very sharp tips has, however, proved difficult. Accordingly, other methods, besides simply sharpening emitter tips, have been proposed for improving electron emission from emitters. Among such other methods are procedures for treating silicon-comprising emitters to convert the silicon to porous silicon, and procedures for treating silicon-comprising field emitters to coat the emitters with materials having lower work function properties than silicon. Such materials include, for example, diamond, cesium (such as, for example, cesiated carbon) and boronitride (the boronitride can be undoped, or doped with, for example, sulfur).

The above-discussed procedures of treating silicon-comprising emitters show promise for improving emission from individual emitters, as well as for improving uniformity of emission across arrays of emitters. Accordingly, it would be desirable to develop methods of fabricating emitters wherein emitter treatments are incorporated into the emitter fabrication processes.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of treating the end portions of an array of substantially upright silicon-comprising structures. A substrate having a plurality of substantially upright silicon-comprising structures extending thereover is provided. The substantially upright silicon-comprising structures have base portions, and have end portions above the base portions. A masking layer is formed over the substrate to cover the base portions of the substantially upright silicon-comprising structures while leaving the end portions exposed. While the masking layer covers the base portions, the end portions are exposed to conditions which alter the end portions relative to the base portions.

In another aspect, the invention encompasses a method of treating the ends of an array of silicon-comprising emitter structures. A substrate having a plurality of silicon-comprising emitter structures thereover is provided. The emitter structures have base portions and ends above the base portions. A layer of spin-on-glass is formed over the substrate. The layer of spin-on-glass covers the base portions of the emitter structures and leaves the ends exposed. While the layer of spin-on-glass covers the base portions, the ends are exposed to conditions which alter the ends relative to the base portions.

In yet another aspect, the invention encompasses a cathode assembly which includes a plurality of silicon-comprising emitter structures projecting over a substrate. The emitter structures have base portions

and ends above the base portions, and the ends comprise a different material than the base portions.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic, cross-sectional, fragmentary view of a portion of an emitter array assembly illustrated at a preliminary step of a method of the present invention.

Fig. 2 is a view of the Fig. 1 assembly shown at a processing step subsequent to that of Fig. 1.

Fig. 3 is a view of the Fig. 1 assembly shown at a processing step subsequent to that of Fig. 2.

Fig. 4 is a view of the Fig. 1 assembly shown at a processing step subsequent to that of Fig. 1 in accordance with a second embodiment method of the present invention.

Fig. 5 is a view of the Fig. 4 assembly shown after a first embodiment treatment process.

Fig. 6 is a view of the Fig. 4 assembly shown after a second embodiment treatment process.

Fig. 7 is a fragmentary, diagrammatic, cross-sectional view of a field emission display incorporating the treated emitters of Fig. 6.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

In one aspect, the invention encompasses methods of treating portions of substantially upright silicon-comprising structures (such as, for example, silicon-comprising emitter structures), while leaving other portions untreated. In particular embodiments, the methodology can be utilized for treating tip regions (i.e., apexes) of silicon-comprising emitter structures, while leaving base regions untreated. Such can advantageously enable modification of electron emitting portions of emitter structures, while not altering physical properties of underlying portions of the emitter structures. Specific embodiments are described with reference to Figs. 1-6.

Referring to Fig. 1, a fragment 10 of a semiconductive material construction is illustrated at a preliminary step of a method of the present invention. Fragment 10 comprises a glass plate 12, a first semiconductive material layer 14 overlying glass plate 12, and emitter structures 20 overlying first semiconductive material layer 14. Emitter structures 20 comprise a second semiconductive material 16. Semiconductive material 14 can comprise either p-type doped or n-type doped semiconductive material, (such as, for example, monocrystalline silicon), and semiconductive material 16 can comprise doped

polycrystalline silicon (polysilicon) material, or, in specific embodiments, consist essentially of conductively doped polysilicon. Materials 12, 14 and 16 together comprise a conventional emitter tip array construction, and can be formed by conventional methods.

To aid in interpretation of this disclosure and the claims that follow, it is noted that layer 14 can be referred to as a "semiconductive substrate". More specifically, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Emitter structures 20 represent a portion of an array of emitter structures. Such array can be referred to as a "cathode array," as the emitters can be incorporated as cathodes in electron emission devices. Each of emitter structures 20 is a substantially upright silicon-comprising structure comprising a base portion 22 and an end portion 24 above the base portion (end portion 24 can also be referred to as an apex, or tip).

A next aspect of the shown exemplary embodiment comprises forming a masking layer over base portions 22 to protect base portions 22 from subsequent conditions. Exemplary methods for forming the masking layer are described with reference to Figs. 2-4, with *Figs. 2*

and 3 illustrating a first embodiment method, and Fig. 4 illustrating a second embodiment method.

Referring to Fig. 2, a masking layer 30 is provided over semiconductive material 14 and over emitter structures 20. Masking material 30 is preferably provided to be thinner over apexes 24 than over base regions 22. Such can be accomplished, for example, by applying material 30 as a liquid. Exemplary processes include applying material 30 through spin-on-glass methodologies, or through so-called "Flowfill™" methodologies. In Flowfill™ methodologies, material 30 is initially provided as silanol (or an organic derivative of silanol). The silanol can be subsequently converted to silicon dioxide through conventional treatment methodologies.

Referring to Fig. 3, material of layer 30 is removed from over apexes 24, but left over base regions 22. In embodiments in which layer 30 comprises either spin-on-glass or silicon dioxide, such can be accomplished by dipping apexes 24 in a hydrofluoric acid-comprising material. For instance, if material 30 comprises spin-on-glass having a thickness of less than 50 Å over apexes 24, the selective removal of material 30 from over apexes 24 can comprise a dip in a hydrofluoric acid solution for about five seconds.

Referring to Fig. 4, another method of applying material 30 over emitters 20 is to utilize conditions which form material of layer 30 only over base regions 22, and not over apexes 24. Such conditions can

include applying material of layer 30 as a liquid, and adjusting the viscosity of such liquid to effectively have the material run off the steep surfaces of apexes 24. The liquid material of layer 30 then collects over layer 14 to a level which covers base regions 22.

Regardless of whether the embodiment of Figs. 2 and 3 is utilized, or the embodiment of Fig. 4 is utilized, the result is a construction having base regions 22 of emitters 20 protected by a masking layer 30, while apexes 24 are exposed through the masking layer 30.

Figs. 5 and 6 illustrate methods of treating apexes 24 with conditions which alter apex regions 24 relative to base regions 22. Fig. 5 illustrates first embodiment processing conditions, and Fig. 6 illustrates second embodiment processing conditions.

Referring to Fig. 5, a low work function material 40 is provided over apex regions 24 and over masking layer 30. The term "low work function" is used herein to refer to materials having lower work functions than material 16. As discussed above, in particular applications material 16 comprises silicon. In such particular applications "low work function" can refer to materials having lower work functions than silicon. In applications in which material 16 comprises silicon, low work function material 40 can comprise, for example, diamond, cesium (such as, for example, cesiated carbon) or boronitride (such as, for example, sulfur doped boronitride). The provision of low work function material 40 over and against apexes 24 can alter electron emission properties of

emitters 20. Specifically, low work function material 40 can increase electron emission across the array of emitters 20. By selectively forming low work function material 40 only against apexes 24, and not against base regions 22, the methodology of the present invention can avoid adversely affecting physical properties of base region 22 with the low work function material of layer 40. Potential adverse effects that could occur if low work function material 40 were provided against base region 22 include spurious electron emission from the base regions of emitters 20. Accordingly, the selective provision of low work function material 40 over only apexes 24 of emitters 20 can form improved emitter devices relative to devices having low work function material provided over an entire surface (i.e., both a base region and an apex region) of an emitter structure.

After formation of low work function material 40 over apexes 24, the construction 10 can be incorporated into, for example, a field emission display device. Masking material 30 and low work function material 40 can be removed from between emitters 20 prior to incorporation in the device. Such removal can be accomplished by, for example, photolithographic processing wherein a photoresist mask is utilized to protect apexes 24 while materials of layers 30 and 40 are etched from between the apexes. Suitable etching conditions can include, for example, HF based solutions or other etchants depending on the low work function material.

Referring to Fig. 6, an alternative method of treating apex regions 24 is illustrated. Specifically, apex regions 24 have been subjected to processing which forms porous silicon (represented by stippling in Fig. 6) within the apex regions. Such formation of porous silicon can increase electron emission and improve uniformity across an array of emitters 20, and can also improve a quality of electron emission from individual emitters 20 of the array. The formation of porous silicon at tip regions 24 can be accomplished by exposing fragment 10 to electrochemical etching in the presence of hydrofluoric acid. During such exposure, layer 30 protects base portions 22 so that apex regions 24 are rendered more porous than base portions 22 by the electrochemical etching. The electrochemical etching procedure can vary depending on whether silicon-comprising material 16 of emitter structures 20 is doped with an n-type material or a p-type material. Specifically, if silicon-comprising material 16 is doped with an n-type material, tip regions 24 are preferably exposed to light during the electrochemical etching. The light can be generated by, for example, a tungsten lamp. If, on the other hand, silicon-comprising material 16 is doped with a p-type material, the electrochemical etching preferably occurs in the dark.

After tip regions 24 have been rendered porous, masking layer 30 can be removed. Methods for removing masking layer 30 can include, for example, photolithographic processing wherein photoresist blocks are formed to protect apex regions 24. Subsequently, the material of

layer 30 that is between apex regions 24 is exposed to etching conditions which remove such material from over silicon-comprising layer 14. The etching conditions can include, for example, HF based solutions or other etchants depending on the masking material.

Fig. 7 illustrates the porous tipped emitter devices 20 of Fig. 6 incorporated into a field emission display device 70. Field emission display device 70 includes dielectric regions 72, spacers 73, an extractor 74, and a luminescent screen 76. Screen 76 is associated with a face plate 80, and emitters 20 are part of a base plate structure 82. Device 70 is constructed with face plate 80 spaced from base plate 82. Techniques for forming field emission displays are described in U.S. Pat. Nos. 5,151,061; 5,186,670 and 5,210,472; hereby expressly incorporated by reference herein.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method of treating portions of an array of substantially upright silicon-comprising structures, comprising:

providing a substrate having a plurality of substantially upright silicon-comprising structures extending thereover, the substantially upright silicon-comprising structures having base portions and end portions above the base portions;

forming a masking layer over the substrate, the masking layer covering the base portions of the substantially upright silicon-comprising structures and leaving the end portions exposed; and

while the masking layer covers the base portions, subjecting the exposed end portions to conditions which alter the end portions relative to the base portions.

2. The method of claim 1 wherein the forming comprises:

depositing the masking layer over the substrate to have a greater thickness over the base portions than over the end portions; and

removing the deposited masking layer from over the end portions to expose the end portions.

3. The method of claim 1 wherein the masking layer comprises spin-on-glass.

4. The method of claim 1 wherein the masking layer comprises silicon dioxide.

5. The method of claim 1 wherein the subjecting comprises subjecting the end portions to conditions which render the end portions more porous than the base portions.

6. The method of claim 5 wherein subjecting comprises electrochemical etching in the presence of HF.

7. The method of claim 5 wherein the silicon of the upright structure is doped with an n-type material, and wherein the subjecting comprises electrochemical etching in the presence of HF and light.

8. The method of claim 5 wherein the silicon of the upright structure is doped with an p-type material, and wherein the subjecting comprises electrochemical etching in the presence of HF.

9. The method of claim 1 wherein the subjecting comprises subjecting the end portions to conditions which cover the end portions with a coating material.

10. The method of claim 9 wherein the coating material comprises a lower work function than silicon.

11. The method of claim 9 wherein the coating material comprises diamond.

12. The method of claim 9 wherein the coating material comprises boron nitride.

13. The method of claim 9 wherein the coating material comprises sulfur-doped boron nitride.

14. The method of claim 9 wherein the coating material comprises cesium.

15. The method of claim 9 wherein the coating material comprises cesiated carbon.

16. A method of treating the ends of an array of silicon-comprising emitter structures, comprising:

providing a substrate having a plurality of silicon-comprising emitter structures thereover, the emitter structures having base portions and ends above the base portions;

forming a layer over the substrate, the layer covering the base portions of the emitter structures and leaving the ends exposed; and

while the layer covers the base portions, subjecting the ends to conditions which alter the ends relative to the base portions.

17. The method of claim 16 wherein the subjecting comprises subjecting the ends to conditions which render the ends more porous than the base portions.

18. The method of claim 17 wherein subjecting comprises electrochemical etching in the presence of HF.

19. The method of claim 17 wherein the silicon of the upright structure is doped with an n-type material, and wherein the subjecting comprises electrochemical etching in the presence of HF and light.

20. The method of claim 17 wherein the silicon of the upright structure is doped with an p-type material, and wherein the subjecting comprises electrochemical etching in the presence of HF.

21. The method of claim 16 wherein the subjecting comprises subjecting the ends to conditions which cover the ends with a coating material.

22. The method of claim 21 wherein the coating material comprises a lower work function than silicon.

23. The method of claim 21 wherein the coating material comprises diamond.

24. The method of claim 21 wherein the coating material comprises boron nitride.

25. The method of claim 21 wherein the coating material comprises sulfur-doped boron nitride.

26. The method of claim 21 wherein the coating material comprises cesium.

27. The method of claim 21 wherein the coating material comprises cesiated carbon.

28. A method of treating the ends of an array of silicon-comprising emitter structures, comprising:

providing a substrate having a plurality of silicon-comprising emitter structures thereover, the emitter structures having base portions and pointed apexes above the base portions;

forming a layer of spin-on-glass over the substrate, the layer of spin-on-glass covering the base portions of the emitter structures and leaving the apexes exposed; and

while the layer of spin-on-glass covers the base portions, subjecting the apexes to conditions which alter the apexes relative to the base portions.

29. The method of claim 28 wherein the subjecting comprises subjecting the apexes to conditions which render the apexes more porous than the base portions.

30. The method of claim 29 wherein subjecting comprises electrochemical etching in the presence of HF.

31. The method of claim 29 wherein the silicon of the upright structure is doped with an n-type material, and wherein the subjecting comprises electrochemical etching in the presence of HF and light.

32. The method of claim 29 wherein the silicon of the upright structure is doped with an p-type material, and wherein the subjecting comprises electrochemical etching in the presence of HF.

33. The method of claim 28 wherein the subjecting comprises subjecting the apexes to conditions which cover the apexes with a coating material.

34. The method of claim 33 wherein the coating material comprises a lower work function than silicon.

35. The method of claim 33 wherein the coating material comprises diamond.

36. The method of claim 33 wherein the coating material comprises boron nitride.

37. The method of claim 33 wherein the coating material comprises sulfur-doped boron nitride.

38. The method of claim 33 wherein the coating material comprises a cesiated carbon film.

39. A method of forming a field emission display device, comprising:

forming a cathode array over a base plate, the cathode array comprising emitter structures having base portions and ends above the base portions;

forming a layer of spin-on-glass over the cathode array, the layer of spin-on-glass covering the base portions of the emitter structures and leaving the ends exposed;

while the layer of spin-on-glass covers the base portions, subjecting the ends to conditions which alter the ends relative to the base portions; and

joining the base plate to a face plate in a configuration wherein the face plate is spaced from the base plate.

40. The method of claim 39 further comprising removing the spin-on-glass from over the base portions prior to joining the base plate to the face plate.

41. The method of claim 39 wherein the spin-on-glass is not removed from over the base portions prior to joining the base plate to the face plate.

42. The method of claim 39 wherein the ends terminate in sharp apexes before the subjecting.

43. The method of claim 39 wherein the subjecting comprises subjecting the ends to conditions which render the ends more porous than the base portions.

44. The method of claim 43 wherein subjecting comprises electrochemical etching in the presence of HF.

45. The method of claim 43 wherein the silicon of the upright structure is doped with an n-type material, and wherein the subjecting comprises electrochemical etching in the presence of HF and light.

46. The method of claim 43 wherein the silicon of the upright structure is doped with an p-type material, and wherein the subjecting comprises electrochemical etching in the presence of HF.

47. The method of claim 39 wherein the subjecting comprises subjecting the ends to conditions which cover the ends with a coating material.

48. The method of claim 47 wherein the coating material comprises a lower work function than silicon.

49. The method of claim 47 wherein the coating material comprises diamond.

50. The method of claim 47 wherein the coating material comprises boron nitride.

51. The method of claim 47 wherein the coating material comprises sulfur-doped boron nitride.

52. The method of claim 47 wherein the coating material comprises cesium.

53. A cathode assembly comprising a plurality of silicon-comprising emitter structures projecting over a substrate, the emitter structures having base portions and ends above the base portions, the ends comprising a different material than the base portions.

54. The assembly of claim 53 wherein the emitter structures comprise conductively doped polysilicon.

55. The assembly of claim 53 wherein the ends terminate in pointed apexes.

56. The assembly of claim 53 wherein the emitter structures consist essentially of conductively doped silicon.

57. The assembly of claim 53 wherein the emitter structures consist essentially of conductively doped polysilicon.

58. The assembly of claim 53 wherein the ends comprise porous silicon and the base portions comprise non-porous silicon.

59. The assembly of claim 53 wherein the ends are coated with a material having a lower work function than silicon and the base portions are not coated with such material.

60. The assembly of claim 59 wherein the material comprises diamond.

61. The assembly of claim 59 wherein the material comprises boron nitride.

62. The assembly of claim 59 wherein the material comprises cesium.

ABSTRACT OF THE DISCLOSURE

In one aspect, the invention encompasses a method of treating the end portions of an array of substantially upright silicon-comprising structures. A substrate having a plurality of substantially upright silicon-comprising structures extending thereover is provided. The substantially upright silicon-comprising structures have base portions, and have end portions above the base portions. A masking layer is formed over the substrate to cover the base portions of the substantially upright silicon-comprising structures while leaving the end portions exposed. The end portions are then exposed to conditions which alter the end portions relative to the base portions. In another aspect, the invention encompasses a method of treating the ends of an array of silicon-comprising emitter structures. A substrate having a plurality of silicon-comprising emitter structures thereover is provided. The emitter structures have base portions and ends above the base portions. A layer of spin-on-glass is formed over the substrate. The layer of spin-on-glass covers the base portions of the emitter structures and leaves the ends exposed. The ends are then exposed to conditions which alter the ends relative to the base portions. In yet another aspect, the invention encompasses a cathode assembly which includes a plurality of silicon-comprising emitter structures projecting over a substrate. The emitter structures have base portions and ends above the base portions, and the ends comprise a different material than the base portions.

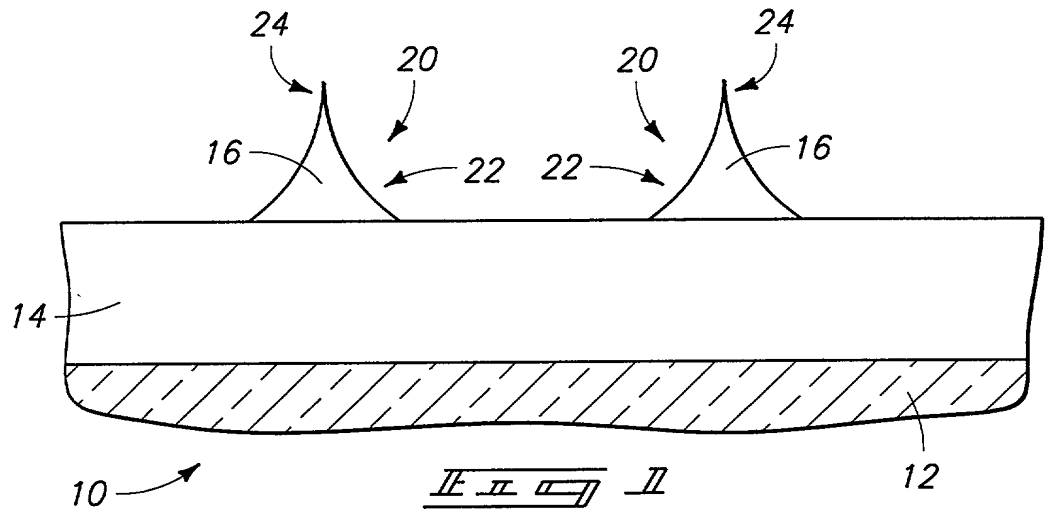

FIG 1

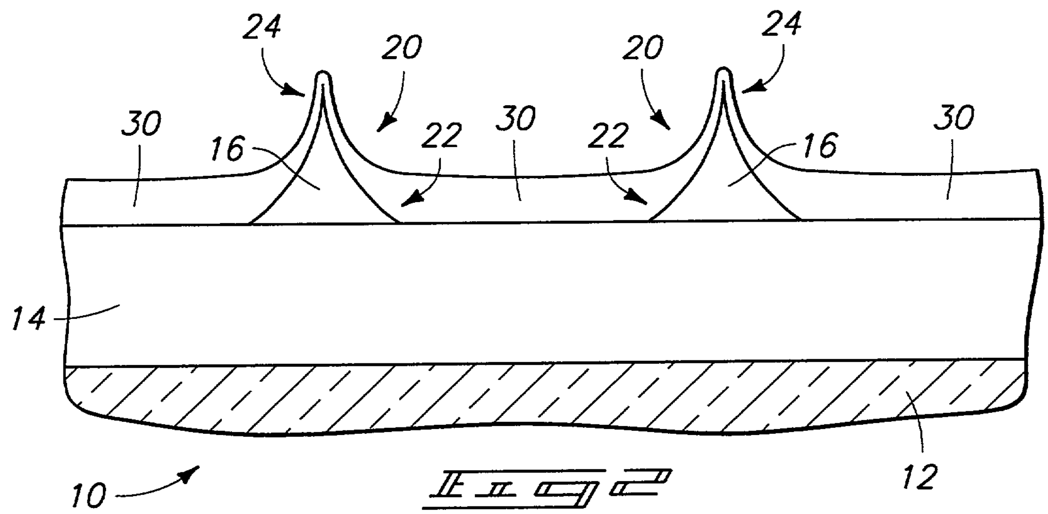

FIG 2

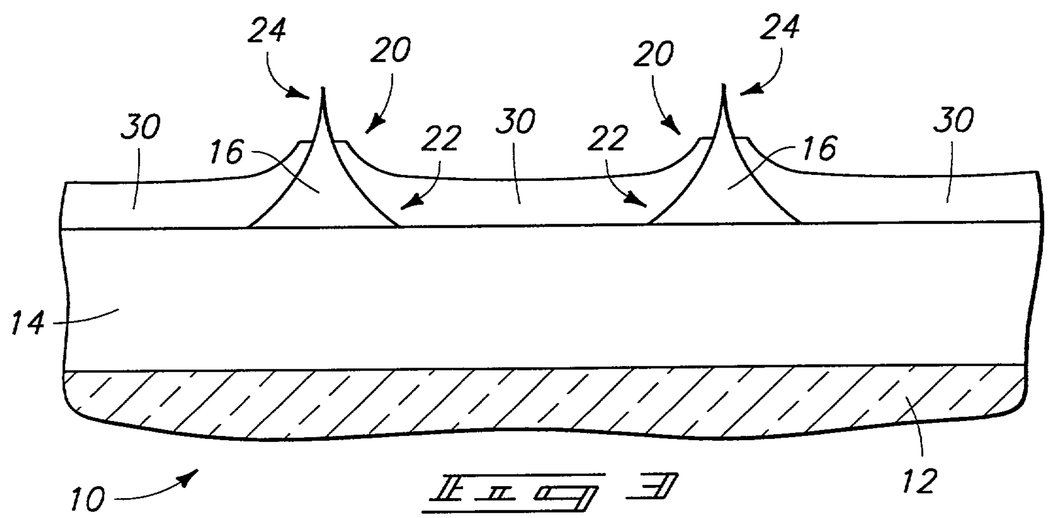

FIG 3

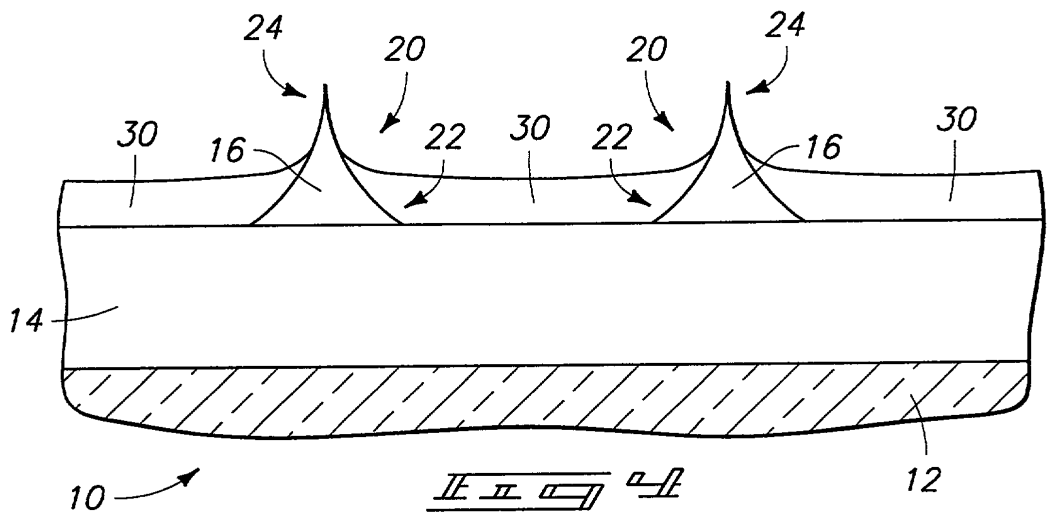

FIG 4

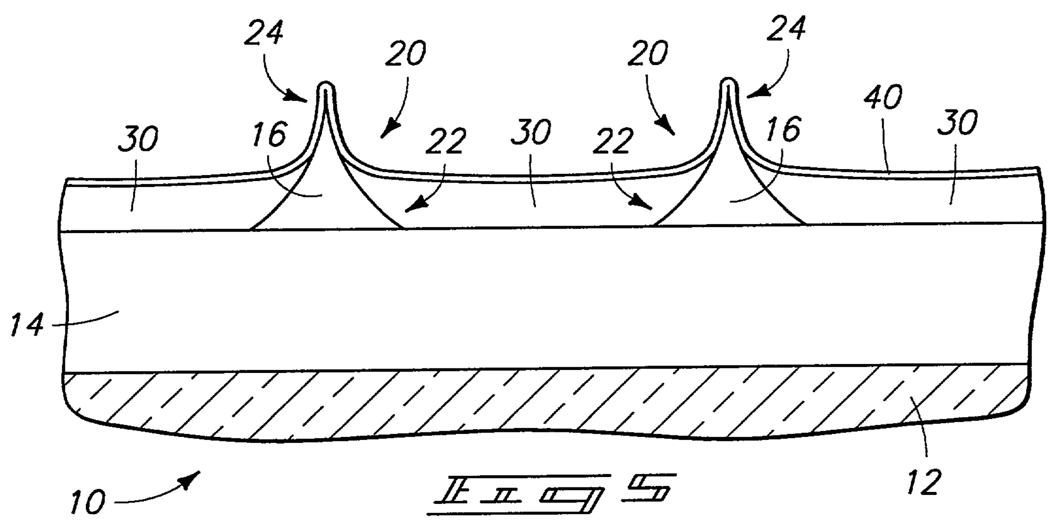

FIG 5

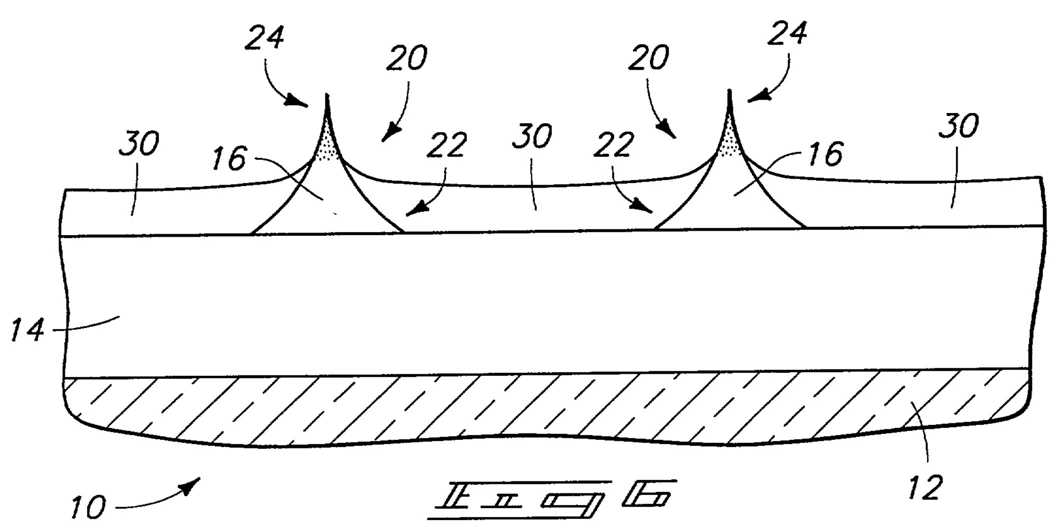

FIG 6

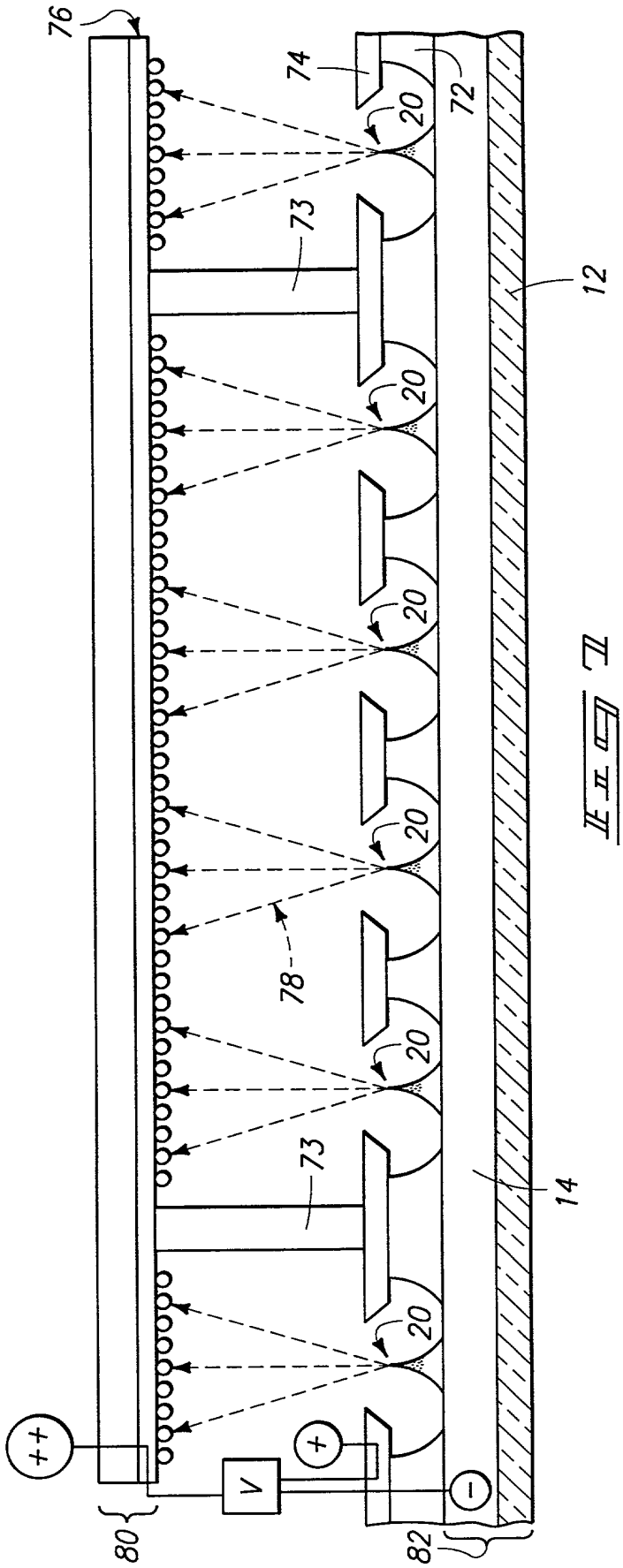

FIG 11

DECLARATION OF SOLE INVENTOR FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods Of Treating Regions Of Substantially Upright Silicon-comprising Structures, Methods Of Treating Silicon-comprising Emitter Structures, Methods Of Forming Field Emission Display Devices, And Cathode Assemblies, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States

Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

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